

What is claimed is:

1. A semiconductor integrated circuit device formed on a semiconductor chip comprising:

an analog voltage processing section for sampling analog voltage in synchronization with a sampling signal and processing the analog voltage;

a PWM driving section for generating a PWM driving signal on the basis of digital processing, to provide a driven section with the PWM driving signal; and

a sampling signal generation circuit for acquiring a variation point of the PWM driving signal from a first level to a second level, wherein the variation point defines a period start point, wherein the variation point is acquired based on a condition that delay time  $t_d$  is shorter than at least a minimum duration of the second level of the PWM driving signal, wherein the delay time  $t_d$  is defined as time from variation of level of the PWM driving signal to actual variation in the passage of current through the driven section, and for providing the analog voltage processing section with a sampling signal at a predetermined point in time when the delay time  $t_d$  elapses from the period start point of the PWM driving signal.

2. The semiconductor integrated circuit device according to claim 1, wherein the sampling signal generation circuit provides the analog voltage processing section with the sampling signal at a point in time when "the delay time  $t_d$  + allowance time  $t_a$ " elapses from the period start point of the PWM driving signal, wherein the delay time  $t_d$  is shorter than "a minimum duration of the second

level - the allowance time  $t_a$ ", and wherein the allowance time  $t_a$  is longer than zero.

3. The semiconductor integrated circuit device according to  
5 claim 2, wherein the PWM driving section outputs the period start point with respect to each period of the PWM driving signal.

4. The semiconductor integrated circuit device according to  
claim 1, wherein the PWM driving section outputs the period start  
10 point with respect to each period of the PWM driving signal.

5. A semiconductor integrated circuit device formed on a semiconductor chip comprising:

an analog voltage processing section for sampling analog  
15 voltage in synchronization with a sampling signal and processing the analog voltage;

a PWM driving section for generating a PWM driving signal on the basis of digital processing and for providing a driven section with the PWM driving signal; and

20 a sampling signal generation circuit for setting reference time  $t_s$  in advance so as to satisfy the following equation:

delay time  $t_d < \text{reference time } t_s \leq (\text{period of PWM driving signal} - \text{delay time } t_d)$

wherein the delay time  $t_d$  is defined as time from variation  
25 of level of the PWM driving signal to actual variation in the passage of current through the driven section,

wherein the sampling signal generation circuit acquires a

variation point of the PWM driving signal from a first level to a second level, the variation point defining a period start point, and also acquires a time width of the second level at the period,

wherein when the reference time  $t_s$  is longer than the duration  
5 of the second level, the sampling signal generation circuit provides the analog voltage processing section with a sampling signal at a point in time when "the reference time  $t_s$  + the delay time  $t_d$ " elapses from the period start point of the PWM driving signal, and

wherein when the reference time  $t_s$  is shorter than the duration  
10 of the second level, the sampling signal generation circuit provides the analog voltage processing section with the sampling signal at a point in time when the reference time  $t_s$  elapses from the period start point.

15 6. The semiconductor integrated circuit device according to claim 5, wherein the sampling signal generation circuit sets the reference time  $t_s$  in advance to satisfy following equation:

(the delay time  $t_d$  + the allowance time  $t_a$ ) < the reference  
time  $t_s \leq$  (the period of PWM driving signal - the delay time  $t_d$  -  
20 the allowance time  $t_a$ )

wherein the allowance time  $t_a$  is greater than zero, to provide the analog voltage processing section with the sampling signal at a point in time when "the reference time  $t_s$  + the delay time  $t_d$  + the allowance time  $t_a$ " elapses from the period start point, when  
25 the reference time  $t_s$  is longer than the duration of the second level.

7. The semiconductor integrated circuit device according to claim 6, wherein the PWM driving section outputs the period start point and the duration of the second level with respect to each period of the PWM driving signal.

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8. The semiconductor integrated circuit device according to claim 5, wherein the PWM driving section outputs the period start point and the duration of the second level with respect to each period of the PWM driving signal.

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9. The semiconductor integrated circuit device according to claim 5, wherein the PWM driving section outputs the period start point a plurality of times during each period of the PWM driving signal so that sampling is performed a plurality of times in each period.

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10. A sampling signal generation circuit for generating a sampling signal for an analog voltage processing section based upon a PWM driving signal generated by a PWM driving section, the sampling signal generation circuit comprising:

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a timing device for acquiring a variation point of the PWM driving signal, the variation point being a transition from a first level to a second level, wherein the variation point is acquired based on a condition that a delay time  $t_d$  is shorter than at least a minimum duration of the second level of the PWM driving signal, wherein the variation point defines a period start point of a PWM period defined by the first level and second level of the PWM driving

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signal, wherein the delay time  $t_d$  is defined as time from variation of level of the PWM driving signal to actual variation in the passage of current through the driven section; and

a comparator for providing the analog voltage processing  
5 section with the sampling signal at a predetermined point in time when the delay time  $t_d$  elapses from the period start point.

11. The sampling signal generation circuit of claim 10,  
wherein the sampling signal generation circuit generates the  
10 sampling signal also based upon the pulse width of the PWM driving signal.

12. The sampling signal generation circuit of claim 11,  
wherein the comparator is further for generating the sampling signal  
15 when an elapsed time from the start point of the PWM period is substantially equal to  $D_e$  when  $D_s$  is more than  $D_p$ , and for generating the sampling signal when the elapsed time is substantially equal to  $D_s$  when  $D_s$  is substantially equal to or less than  $D_p$ , wherein  $D_e$  is representative of a summation of a reference time  $t_s$ , the  
20 delay time  $t_d$  and an allowance time  $t_a$ , wherein  $D_s$  is representative of a summation of the reference time  $t_s$  and wherein  $D_p$  is representative of the pulse width of the PWM driving signal.

13. The sampling signal generation circuit of claim 10,  
25 wherein the sampling signal generation circuit generates the sampling signal a plurality of times in each PWM period.